Docket No.: 20136-00305-US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Roy C. (deceased), Flaker et al.

Application No.: 09/588,351 | Confirmation No.: 8116

Filed: June 7, 2000 | Art Unit: 2815

For: CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES | Examiner: J. A. Fenty

APPELLANT'S BRIEF UNDER 37 C.F.R. § 1.192

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notice of Appeal filed on June 18, 2004, the undersigned hereby submits this Brief on Appeal Under 37 C.F.R. § 1.192.

The fees required under § 1.17(f) and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief is transmitted in triplicate.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

I. Real Party In Interest

The real party in interest is the International Business Machines Corporation, Assignee of the present application.

II Related Appeals and Interferences

There are no related appeals or interferences known to the undersigned which will directly effect or be directly effected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims

Claims 1-5 have been cancelled.

Claims 6-14 are pending in the application.

Claim 15 is withdrawn from consideration.

Claims 6-14 are rejected and are on appeal.

IV. Status of Amendments

There are no unentered amendments filed subsequent to the Final Rejection.

V. Summary of Invention

The invention provides a method for enhancing the performance of an SOI device. As shown in FIG. 2, an SOI device includes a substrate 210, and an insulating layer 220. Devices are fabricated above the insulation layer 220. The advantage of the structure is disclosed in the specification, particularly on page 2 beginning at line 18 thereof, wherein SOI devices are described as typically having lower parasitic capacitances. This means that SOI devices can provide faster switching times. As described on page 3 beginning at line 21, the SOI device can accumulate electric charge on the body (the region of the MOSFET between the source and the drain). The increased charge can adversely effect the operation of the circuit, notably switching speed.

The present invention, as embodied in the circuit of FIG. 3 provides for discharging this accumulated charge. In operation, transistor 360 acts as a switch interconnecting circuits 320 and 330 whenever operation signal 350 is activated. The pulse discharge circuit 310 enhances the switching speed of transistor 360, by, just prior to activating the operation signal 350, discharging the accumulated charge from transistor 360 to reference ground 370.

FIG. 6 shows a practical embodiment wherein word line drivers 430, 440 are discharged prior to accessing a word line. When the segment driver 450 is activated, the same control signal (CTL) is used to select one of the memory subarrays or segments for writing, and is also used as an input to the pulse discharge circuit 310. The activated pulse discharge circuit 310 pulls each of transistors 432, 435, etc. to a reference ground discharging the accumulated charge on the memory subarray just prior to selection of the subarray for access. The foregoing initializes the subarray so that it can be accessed at a greater speed.

VI. Issues

The issues on appeal are:

1. Are claims 6-14 properly rejected under 35 U.S.C. § 102(e) as being anticipated by Okumura et al. (U.S. Pat. No. 5,892,260); and

2. Are claims 6-14 properly rejected under the judicially created doctrine of double obviousness type double patenting as being unpatentable over claims 1-4 of Flaker et al. (U.S. Pat. No. 6,160,292) in view of Okumura et al. (U.S. Pat. No. 5,892,260)?

VII. Grouping of Claims

Claims 6-7 and 9-12 stand and fall together.

Claim 8 stands and falls alone.

Claims 9 and 10 stand and fall together.

VIII. Arguments

The Rejection of Claims 6-14 Under 35 U.S.C. § 102(e) is in error

The present invention is directed to a method for enhancing the performance of an SOI semiconductor device. It is possible for a charge to accumulate on the body of SOI devices which reduces there switching speed. In accordance with the Applicants rejected claim 6, circuit performance is enhanced by the steps of a) providing a pulse discharge circuit connected to at least one SOI device, and b) using the pulse discharge circuit to discharge any accumulated potential on a body of at least one SOI device prior to accessing the at least one SOI device. Thus, the method step calls for discharging of the SOI device prior to accessing it, so that the speed of switching can be maximized.

The Okumura et al. (U.S. Pat. No. 5,892,260) patent fails to disclose the claimed process. Okumura et al. does not disclose any type of pulse discharge circuit, nor does it dispose that feature of Applicants method claim which requires that the body be discharged prior to access.

Okumura et al. (U.S. Pat. No. 5,892,260) provides for a bias voltage generator 312 to bias the back gate region of a P-channel transistor to the supply voltage V_{DD}. This increases the absolute value of the threshold voltage for the device, and when the active mode is entered, the bias voltage generating circuit causes a voltage of the back gate region 305 to be at a voltage V_1 which is lower than V_{DD} and higher than V_{DD}-V_F. The result is a decrease in the absolute value of the threshold (see in particular col. 6, lines 17-27). There is no effective way of discharging the body of the device prior to access. The reference fails to disclose anywhere the advantages of discharging any accumulated potential on the body of an SOI device. Accordingly, the feature of Applicants claimed method that requires accumulated potential to be discharged prior to accessing the SOI device is not suggested in the reference. It is submitted that biasing the substrate of a device in a standby mode for minimizing power dissipation, and for lowering a threshold voltage in an active mode such that it responds to a rapid switching signal, are not identical to discharging potential on a body before accessing an SOI device.

The entire thrust of the Okumura et al. (U.S. Pat. No. 5,892,260) invention summarized in col. 4, lines 5-14 as follows:

> The threshold voltage V_{thn} is dependent upon a back gate voltage, i.e., the substrate voltage V_{subn}, as shown in FIG. 2. That is, the higher the substrate voltage V_{subn}, the lower the threshold voltage V_{thn}. Therefore, in an active mode, the substrate voltage V_{subn} is positive to lower the threshold voltage V_{thn}, so that the operation speed is increased and the power dissipation is increased. On the other hand, in a standby mode, the substrate voltage V_{subn} is zero to raise the threshold voltage V_{thn}, so that the sub threshold current is decreased to decrease the power dissipation and the operation speed is decreased.

The foregoing process does not seek to reduce any accumulated charge, as is provided by the pulse generator in accordance with the present invention. Since the subject matter of the reference is directed to portable electronic apparatus, and conserving power, the standby mode is used with the voltage biasing to reduce power consumption in the standby mode. The switching from a standby mode to an active mode, does not suggest a pulse generation technique which discharges accumulated charge prior to switching the SOI device.

Claim 8 includes a further limitation which is not shown in Okumura et al. (U.S. Pat. No. 5,892,260). Specifically, claim 8 requires a delay element be coupled to the input signal. An output signal coupled to the input signal drives the circuit operation. Thus, the circuit operation is delayed until such time as the body of the device can be discharged. The use of the delay element for making certain that the circuit is initialized, by discharging accumulated charge, is not shown or disclosed in Okumura et al. (U.S. Pat. No. 5,892,260).

Claim 9 includes the limitations of selectively grounding at least on the plurality of SOI devices. This process step is also not shown or disclosed in the cited reference.

Rejection of Claims 6-14 Under the Judicially Created Doctrine of Obviousness Type Double Patenting as being Unpatentable over Claims 1-4 of Flaker et al. (U.S. Pat. No. 6,160,292) in view of Okumura et al. (U.S. Pat. No. 5,892,260) is in error.

As can be seen from FIG. 6, a method is described which uses a pulse discharge circuit to discharge any accumulated potential on at least one SOI device *prior* to accessing the at least one SOI device. The foregoing step of discharging the accumulated potential prior to accessing the device is not seen in the claims of the Flaker et al. (U.S. Pat. No. 6,160,292) patent. Further, the claims of the Flaker et al. (U.S. Pat. No. 6,160,292) patent require that the plurality of SOI devices be discharged, and not selective ones as set forth in claim 9.

The reference to Okumura et al. (U.S. Pat. No. 5,892,260) also does not disclose these limitations, which would result in rendering obvious the rejected claims. As it has been noted, Okumura et al. (U.S. Pat. No. 5,892,260) fails to disclose the discharge of an SOI device, as well as the discharge of the SOI device prior to accessing the SOI device.

IX. Summary

The Final Rejection fails to make a *prima facie* case of obviousness under 35 U.S.C. § 102, or 35 U.S.C. § 103. Under 35 U.S.C. § 102, a claim is anticipated only if each and every element as set forth in the claim is found either expressly or inherently described in a single prior art reference. As has been shown above, the claims are not anticipated since not every element can be found in the cited patent to Okumura et al. (U.S. Pat. No. 5,892,260).

The judicially created doctrine of obviousness type double patenting requires the rejection of an application when the claimed subject matter is not patentably distinct from the subject matter claimed in the commonly owned patent, when the issuance of a second patent would provide unjustified extension of the term of the right to exclude granted by a patent (MPEP Section 804 citing Eli Lilly and Company, v. Bar Labs, Inc. 251F3rd. 955, 58 USPQ2nd 1865 (Fed. Cir. 2001); Ex party Davis 56 USPQ2nd 1434, 1435-36 (Board of Patent Appeals and Interferences 2000). The analysis employed in an obviousness type double patenting determination parallels the guidelines for a 35 U.S.C. § 103(a) rejection. The claims of the prior patent must, when combined with the secondary reference result in a *prima facie* case of obviousness. As set forth above, any such combination does not yield or suggest all the comments of Applicants claims and therefore no *prima facie* case of obviousness is established.

X. Claims Involved In The Appeal

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A do include the amendments filed by Applicant on April 26, 2004.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 09-0458, under Order No. 20136-00305-US from which the undersigned is authorized to draw.

Dated: August 18, 2004

Respectfully submitted,

By _____

George R. Pettit, Reg. No. 27,369
CONNOLLY BOVE LODGE & HUTZ LLP
1990 M Street, N.W., Suite 800
Washington, DC 20036-3425
(202) 331-7111
(202) 293-6229 (Fax)
Attorney for Applicant

APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/588,351

6. (Previously presented) In a circuit comprising at least one SOI device, a method for enhancing the performance of the circuit, the method comprising the steps of:

providing a pulse discharge circuit connected to the at least one SOI device;

using the pulse discharge circuit to discharge any accumulated potential on a body of the at least one SOI device prior to accessing the at least one SOI device.

7. (Original) The method of claim 6 wherein the circuit comprises a memory circuit.

8. (Original) The method of claim 6 wherein the pulse discharge circuit comprises:

an input signal;

a delay element coupled to the input signal; and

an output signal coupled to the input signal, the output signal driving the circuit.

9. (Previously presented) In a circuit comprising a plurality of SOI devices, wherein each of the plurality of SOI devices has a body, a method for enhancing the performance of the circuit, the method comprising the step of:

selectively grounding the body of at least one of the plurality of SOI devices to dissipate an electric charge accumulated in the body of the at least one of the plurality of SOI devices before accessing said SOI devices.

10. (Original) The circuit of claim 9 wherein the plurality of SOI devices comprises a memory circuit.

11. (Previously presented) In a circuit comprising a plurality of SOI devices, wherein each of the plurality of SOI devices has a body, a method for enhancing the performance of the circuit, the method comprising:

providing a pulse discharge circuit, the pulse discharge circuit having a pulse generator connected to the circuit;

using the pulse generator to generate a pulse;

discharging any accumulated potential on the body of at least one of the plurality of SOI devices to a point having a lower potential than the accumulated potential of the body in response to the pulse from the pulse generator prior to accessing said at least one SOI devices.

12. (Original) The method of claim 11 wherein the plurality of SOI devices comprises a memory circuit.

13. (Original) The method of claim 12 wherein the pre-determined time is just prior to accessing the memory circuit for reading or writing data.

14. (Previously presented) A method for discharging accumulated charge from a body of an SOI device and accessing the SOI device, comprising:

generating a pulse;

using the generated pulse to provide a conductive path from the body of the SOI device to a reference point having a lower potential than the accumulated charge;

discharging the accumulated charge from the body of the SOI device to the reference point;

providing a control signal which enables access to the SOI device; and

reading an output of the SOI device,

wherein said steps of generating a pulse and discharging the accumulated charge occur prior to said step of reading an output of the SOI device.

IFW
AF

TRANSMITTAL OF APPEAL BRIEF	Docket No. 20136-00305-US

In re Application of: Roy C. (deceased), Flaker et al.

Application No.	Filing Date	Examiner	Group Art Unit
09/588,351-Conf. #8116	June 7, 2000	J. A. Fenty	2815

Invention: CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed: June 18, 2004 .

The fee for filing this Appeal Brief is 330.00 .

- [x] Large Entity - [ ] Small Entity

- [ ] A check in the amount of ______________ is enclosed.

- [x] Charge the amount of the fee to Deposit Account No. 09-0458 .
  This sheet is submitted in duplicate.

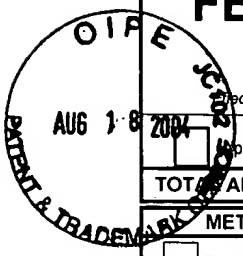
- [ ] Payment by credit card. Form PTO-2038 is attached.

- [x] The Director is hereby authorized to charge any additional fees that may be required or credit any overpayment to Deposit Account No. 09-0458 .
  This sheet is submitted in duplicate.

Dated: August 18, 2004

George R. Pettit
Attorney Reg. No. : 27,369
CONNOLLY BOVE LODGE & HUTZ LLP
1990 M Street, N.W., Suite 800
Washington, DC 20036-3425
(202) 331-7111

PTO/SB/17 (10-03)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	09/588,351-Conf. #8116
Filing Date	June 7, 2000
First Named Inventor	Roy C. (deceased), Flaker
Examiner Name	J. A. Fenty
Art Unit	2815
Attorney Docket No.	20136-00305-US

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit Card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 09-0458

Deposit Account Name: IBM Corporation (Fishkill)

The Director is authorized to: *(check all that apply)*

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		-** =		x		=	
Independent Claims		-** =		x		=	
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
Other fee (specify)					

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($) 330.00

SUBMITTED BY

(Complete *(if applicable)*)

Name (Print/Type)	George B. Pettit	Registration No. (Attorney/Agent)	27,369	Telephone	(202) 331-7111
Signature				Date	August 18, 2004